14/5/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

06629288 **Image available**
ADVANCED MEMORY HIERARCHICAL STRUCTURE FOR PROCESSOR

PUB. NO.: 2000-215102 [JP 2000215102 A]
PUBLISHED: August 04, 2000 (20000804)
INVENTOR(s): SANJIVE AGARWALA
BOSSHART PATRICK W
ANDERSON TIMOTHY
APPLICANT(s): TEXAS INSTR INC (TI)
APPL. NO.: 11-287163 [JP 99287163]
FILED: September 01, 1999 (19990901)
PRIORITY: 98797 [US 9898797], US (United States of America), September 01, 1998 (19980901)
INTL CLASS: G06F-012/08

ABSTRACT

PROBLEM TO BE SOLVED: To shorten the time needed for memory access by including cache levels for data, instructions, and integrated data and instructions.

SOLUTION: The microprocessor 10 has three levels of its internal cache memories. A **level - 2** cache 14 of the highest order is an integrated cache and stores codes and data and receives all data and instructions which can be cached from a data processing system 2 through a bus interface unit 12 from a bus B. The **level - 2 cache** 14 is connected to **two level - 1 caches** 16. A **level - 1** data **cache** 16d is used exclusively for data and a **level - 1** instruction cache 16i is used exclusively for instructions. Further, a level-0 cache 18 is provided on a data side. In the microprocessor 10, a multiple execution unit is provided and executes up to four instructions at the **same time** in **parallel** .

14/5/2 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

06417749 **Image available**
OVERLAPPED MEMORY ACCESS METHOD AND DEVICE TO **L1** AND **L2**

PUB. NO.: 2000-003308 [JP 2000003308 A]
PUBLISHED: January 07, 2000 (20000107)
INVENTOR(s): DHONG SANG H
HALM PETER HOFSTAY
MELTZER DAVID
JOEL ABRAHAM SILVERMAN
APPLICANT(s): INTERNATL BUSINESS MACH CORP (IBM)
APPL. NO.: 11-096228 [JP 9996228]
FILED: April 02, 1999 (19990402)
PRIORITY: 59000 [US 9859000], US (United States of America), April 13, 1998 (19980413)
INTL CLASS: G06F-012/08

ABSTRACT

PROBLEM TO BE SOLVED: To provide a method for realizing **simultaneous** , memory overlapped access to **plural cache levels** to reduce the waiting time or penalty of an upper level cache mistake.
SOLUTION: The demand of a value (data or an instruction) is issued by a process 104 and is transferred to a lower level cache before it is decided whether a cache mistake of the value is generated at a cache of an upper level. In an execution configuration in which a lower level is an **L2** cache, it is possible to directly supply a processor with a value. An address decoder operates at the upper **level cache** in **parallel** and can

priority **plural simultaneous** memory demands. One of addresses (selected in order of priority logic on the basis of hit-miss information from the upper level cache) is gated to a work line driver of a memory array of the cache at the lower level by a multiplexer. Several bits among the address which do not need conversion from virtual into real can be immediately decoded.

14/5/3 (Item 1 from file: 350)

015644980 **Image available**
WPI Acc No: 2003-707163/200367
Related WPI Acc No: 2003-028294
XRPX Acc No: N03-564881

Data processing system for multiprocessor environment, prefetches predetermined stream of cache lines concurrently into different levels of caches , using prefetch engine

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: KAHLE J A; MAYFIELD M J; O'CONNELL F P; RAY D S; SILHA E J; TENDLER J M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6574712	B1	20030603	US 99435865	A	19991108	200367	B
			US 2000550180	A	20000414		

Priority Applications (No Type Date): US 2000550180 A 20000414; US 99435865 A 19991108
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6574712	B1		15	G06F-012/08	CIP of application US 99435865 CIP of patent US 6460115

Abstract (Basic): US 6574712 B1

NOVELTY - An overriding circuitry overrides a prefetch engine (202), in response to a single instruction executed in the processor, so as to prefetch a predetermined stream of cache lines **concurrently** into on-chip caches (**L1**) and larger off-chip caches (**L2** , **L3**).

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(1) multiprocessor system; and

(2) method for prefetching data with respect to several cache levels.

USE - For multiprocessor environment.

ADVANTAGE - By implementing several cable levels, memory latencies associated with increasing processor speeds are reduced and the prefetching for the lower memory hierarchy within a **multilevel cache** system is performed without burdening the data buses with prefetch traffic.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the hardware prefetch mechanism.

prefetch engine (202)

pp; 15 DwgNo 2/11

Title Terms: DATA; PROCESS; SYSTEM; MULTIPROCESSOR; ENVIRONMENT; PREDETERMINED; STREAM; CACHE; LINE; **CONCURRENT** ; LEVEL; ENGINE
Derwent Class: T01
International Patent Class (Main): G06F-012/08
File Segment: EPI

14/5/4 (Item 2 from file: 350)

015095632 **Image available**
WPI Acc No: 2003-156150/200315
XRPX Acc No: N03-123247
Multiprocessor system has higher- level caches **each supporting** multiple concurrent **invalidations of lines within the cache**
Patent Assignee: SUN MICROSYSTEMS INC (SUNM); CHAUDHRY S (CHAU-I); TREMBLAY M (TREM-I)
Inventor: CHAUDHRY S; TREMBLAY M
Number of Countries: 101 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020152359	A1	20021017	US 2001283252	P	20010411	200315	B
			US 200261493	A	20020131		
WO 200284494	A2	20021024	WO 2002US11561	A	20020411	200315	
EP 1377908	A2	20040107	EP 2002719499	A	20020411	200404	
			WO 2002US11561	A	20020411		

Priority Applications (No Type Date): US 2001283252 P 20010411; US 200261493 A 20020131
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020152359	A1		14	G06F-013/00	Provisional application US 2001283252

WO 200284494 A2 E G06F-012/08
Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW
EP 1377908 A2 E G06F-012/08 Based on patent WO 200284494
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR

Abstract (Basic): US 20020152359 A1
NOVELTY - A lower-level cache (**L2**) (106) includes several banks (202-205) that are accessible in **parallel** to support **multiple concurrent** operations. Several higher- **level caches** (**L1**) (112,122,132,142) connected to processors (110,120,130,140), perform memory accesses through the **L2** cache. Each **L1** cache supports multiple **concurrent** invalidations of lines within the **L1** cache.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for the following:
(1) Multiple cache line invalidation supporting cache; and
(2) Multiple cache line invalidation method.
USE - Multiprocessor system.
ADVANTAGE - Enables **concurrent** invalidations of several entries in an **L1** cache within a single cycle without performing a look-up to determine the location of the entry.
DESCRIPTION OF DRAWING(S) - The figure illustrates the **L2** cache with multiple banks within multiprocessor system.
Processors (110,120,130,140)
L1 caches (112,122,132,142)
L2 cache (106)
Banks of **L2** cache (202-205)
pp; 14 DwgNo 2/7
Title Terms: MULTIPROCESSOR; SYSTEM; HIGH; LEVEL; SUPPORT; MULTIPLE; **CONCURRENT** ; LINE; CACHE
Derwent Class: T01; U14
International Patent Class (Main): G06F-012/08; G06F-013/00
File Segment: EPI

14/5/5 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014903303 **Image available**
WPI Acc No: 2002-724009/200278
XRPX Acc No: N02-570854

Multiprocessor system for computer cache access using lower level cache to perform lookup in reverse directory to find target entry in higher level cache

Patent Assignee: CHAUDHRY S (CHAU-I); TREMBLAY M (TREM-I); SUN MICROSYSTEMS INC (SUNM)
Inventor: CHAUDHRY S; TREMBLAY M
Number of Countries: 100 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200284492	A2	20021024	WO 2002US11560	A	20020411	200278	B
US 20020178329	A1	20021128	US 2001283254	P	20010411	200281	
			US 200261502	A	20020131		
US 6634297	B2	20040127	US 2001283254	P	20010411	200408	
			US 200261502	A	20020131		

Priority Applications (No Type Date): US 200261502 A 20020131; US 2001283254 P 20010411
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200284492	A2	E	25	G06F-012/00	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VN YU ZA ZM ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SL SZ TR TZ UG ZM ZW

US 20020178329	A1	G06F-012/08	Provisional application	US 2001283254
US 6634297	B2	G06F-012/08	Provisional application	US 2001283254

Abstract (Basic): WO 200284492 A2

NOVELTY - **Multi** -processor system comprises processors, a lower **level cache** , higher level caches configured to perform memory accesses through the lower level cache, and a reverse directory coupled to the lower level cache which includes entries for lines in the higher level caches identifying an associated entry in the lower level cache.

DETAILED DESCRIPTION - The low-level cache is configured to receive requests from a higher level cache to retrieve a line from the lower level cache and if the line is present it sends the line to the higher level cache so that it can be stored there and stores information in the reverse directory to indicate that the line is stored in a high-level cache. The lower level cache also receives an update request that causes a target entry in the lower-level cache to be updated and performs a look-up in the reverse directory to determine if the target entry is contained in a higher level cache. For each higher level cache that contains the target entry it sends an invalidation request to high-level cache and updates the corresponding entry in the reverse directory to indicate that the target entry has been invalidated in the higher level cache. The reverse directory includes a fixed entry corresponding to each entry in each higher **level cache** , the **multi** -processor system is located on a single semiconductor chip, the lower level cache is an **L2** cache and each higher level cache is an **L1** cache. The higher level caches are organized as write-through **caches** and the lower- **level cache** has **multiple** banks that can be accessed in **parallel** . There are INDEPENDENT CLAIMS for:

(1) A single-chip multiprocessor system

(2) A method of data access through a lower-level cache

USE - Multiprocessor system is for using a reverse directory located at a lower-level cache to facilitate operations involving higher-level caches that perform accesses through the lower-level cache.

ADVANTAGE - System maintains directory information for **L1** caches without wasting memory and invalidates an entry in an **L1** cache without performing a lookup to determine the way location of the entry.

DESCRIPTION OF DRAWING(S) - The figure shows a reverse directory.
pp; 25 DwgNo 3/6
Title Terms: MULTIPROCESSOR; SYSTEM; COMPUTER; CACHE; ACCESS; LOWER; LEVEL; CACHE; PERFORMANCE; REVERSE; DIRECTORY; FINDER; TARGET; ENTER; HIGH; LEVEL; CACHE
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-012/08
File Segment: EPI

14/5/6 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014345009 **Image available**
WPI Acc No: 2002-165712/200222
Related WPI Acc No: 2001-376794; 2001-376796; 2001-383384; 2002-165714; 2003-089239; 2003-729705
XRPX Acc No: N02-126537
Intensive numeric algorithm processor for cellular mobile telephone, has Digital Signal Processor with dual load/store units connected to dual memory ports in level one cache
Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: ANDERSON T D; HOYLE D; STEISS D E; KRUEGER S D
Number of Countries: 028 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1126368	A2	20010822	EP 200122	A	20010219	200222	B
JP 2001256105	A	20010921	JP 200142414	A	20010219	200222	
US 6539467	B1	20030325	US 99165512	P	19991115	200325	
			US 2000183417	P	20000218		
			US 2000183527	P	20000218		
			US 2000703105	A	20001031		

Priority Applications (No Type Date): US 2000703105 A 20001031; US 2000183417 P 20000218; US 99165512 P 19991115; US 2000183527 P 20000218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1126368	A2	E	41	G06F-009/34	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR					
JP 2001256105	A		34	G06F-012/04	
US 6539467	B1			G06F-012/00	Provisional application US 99165512 Provisional application US 2000183417 Provisional application US 2000183527

Abstract (Basic): EP 1126368 A2
NOVELTY - The Digital Signal Processor (DSP) (1301) has instruction set architecture (ISA) designed for intensive numeric algorithm processing using dual load/store units (D1, D2) connected to **dual** memory ports (T1, T2) in **level one cache** memory controller (1720a). The DSP can execute two aligned data transfers each having a length of one, two, four or eight bytes in **parallel** by executing two load/store instructions.
DETAILED DESCRIPTION - The DSP can also execute a single non-aligned data transfer having a length of four or eight bytes executing a non-aligned load/store instruction that utilizes both memory target ports.
An INDEPENDENT CLAIM is included for a method of operating a microprocessor.
USE - For use in the DSP of a cellular telephone.
ADVANTAGE - Improved processing in a cellular telephone by using a DSP with **parallel** processing architecture.
DESCRIPTION OF DRAWING(S) - The block diagram represents a digital processing system for use in a cellular telephone.
Digital Signal Processor (1301)
Cache memory controller (1720a)

Dual load/store units (D1, D2)
dual memory ports (T1, T2)
pp; 41 DwgNo 13/14
Title Terms: INTENSE; NUMERIC; ALGORITHM; PROCESSOR; CELLULAR; MOBILE; TELEPHONE; DIGITAL; SIGNAL; PROCESSOR; DUAL; LOAD; STORAGE; UNIT; CONNECT; DUAL; MEMORY; PORT; LEVEL; ONE; CACHE
Derwent Class: T01; W01
International Patent Class (Main): G06F-009/34; G06F-012/00; G06F-012/04
International Patent Class (Additional): G06F-009/312; G06F-009/38
File Segment: EPI

14/5/7 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014066567 **Image available**
WPI Acc No: 2001-550780/200162
XRPX Acc No: N01-409155

Cache address conflict device without storage buffer for computer systems, has plane of multi-level/plane structure provided with a queue for holding entries of address information for data access

Patent Assignee: HEWLETT-PACKARD CO (HEWP); INTEL CORP (ITLC)
Inventor: GRUTKOWSKI T; MULLA D A; RIEDLINGER R J
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10045188	A1	20010906	DE 1045188	A	20000913	200162	B
US 6539457	B1	20030325	US 2000510279	A	20000221	200325	

Priority Applications (No Type Date): US 2000510279 A 20000221
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10045188	A1		17	G06F-012/08	
US 6539457	B1			G06F-012/00	

Abstract (Basic): DE 10045188 A1

NOVELTY - To extend the capability of conventional caches beyond being able to handle only a limited number of requests **simultaneously** as a result of the serial structure of these conventional **caches** , a **multi - level** /plane structure is used for memory access requests to be carried out, and is configured in order that the several planes/levels can receive several memory access requests, which are then **parallel** -processed. A plane or level of the multi-plane/level structure has a queue for holding entries of address information for data access and includes a conflict logic for testing each access request with regard to the entries of the queue for conflicts before insertion of each access request into the queue. An output logic decides which entries are to be outputted from the waiting queue as based on the results of the conflict logic.

USE - Computer systems and especially cache memory systems.

ADVANTAGE - The computer system has a simplified storage buffer structure with low surface area demand.

DESCRIPTION OF DRAWING(S) - A Block diagrammatic arrangement of the inventive cache arrangement is given.(Contains non-English language text).

L1 -cache (101)
L0-command cache (102)
L0-data cache (103)
CPU-core (104)
Bus (106)
Four gates (107)
Two gates (108)
Four gates (109)
Data feedback bus (111)
Bus (113)
Path (114)
pp; 17 DwgNo 1/7

Title Terms: CACHE; ADDRESS; CONFLICT; DEVICE; STORAGE; BUFFER; COMPUTER; SYSTEM; PLANE; MULTI; LEVEL; PLANE; STRUCTURE; QUEUE; HOLD; ENTER; ADDRESS; INFORMATION; DATA; ACCESS
Derwent Class: T01
International Patent Class (Main): G06F-012/00; G06F-012/08
File Segment: EPI

14/5/8 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014051685 **Image available**
WPI Acc No: 2001-535898/200159
XRPX Acc No: N01-397996
Graphics processing method for computer system, involves updating cache flags associated with each of cache lines of cache **, based on data availability in each of** level one **and** level two caches
Patent Assignee: S3 INC (STHR-N)
Inventor: FU C; HSU H; LING I
Number of Countries: 020 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200120460	A1	20010322	WO 2000US25245	A	20000914	200159	B

Priority Applications (No Type Date): US 99399280 A 19990917
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200120460	A1	E	45	G06F-012/08	

Designated States (National): CA JP
Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
Abstract (Basic): WO 200120460 A1
NOVELTY - **L2** and **L1** caches (13,15) are respectively comprised of cache lines. Availability of graphics data in each of the **L2** and **L1** caches, is checked. Based on availability of graphics data in caches (13,15), cache flags associated with each of cache lines of cache (13), are updated. Cache flags associated with each of cache lines of cache (15) are updated, based on availability of graphics data in the cache (15).
DETAILED DESCRIPTION - The cache lines of **L2** cache are divided into several slots and are also divided into several sets. The cache flags associated with each of cache lines of cache (13) have several reference counters. INDEPENDENT CLAIMS are also included for the following:
(a) Graphics processing system;
(b) **Synchronized two level cache** system
USE - For **synchronization** of **two level cache** in graphics processing system for computer system.
ADVANTAGE - Reduces memory access time, by transferring appropriate portions of texture map between **level one** and **level two caches**.
DESCRIPTION OF DRAWING(S) - The figure shows the system block diagram of computer system.
L2 and **L1** caches (13,15)
pp; 45 DwgNo 1/15
Title Terms: GRAPHIC; PROCESS; METHOD; COMPUTER; SYSTEM; UPDATE; CACHE; FLAG; ASSOCIATE; CACHE; LINE; CACHE; BASED; DATA; AVAILABLE; LEVEL; ONE; LEVEL; TWO
Derwent Class: T01
International Patent Class (Main): G06F-012/08
File Segment: EPI

14/5/9 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014036067 **Image available**
WPI Acc No: 2001-520280/200157
Related WPI Acc No: 1998-495146; 1998-567879; 1999-008947; 2000-505556; 2000-542917; 2001-289595
XRPX Acc No: N01-385262

Clock signal generation system has reset counter that provides synchronization between phase locked loops, after shifting core clock signal

Patent Assignee: INTEL CORP (ITLC)
Inventor: BARKATULLAH J S; FISCH M A; PATHIKONDA C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6268749	B1	20010731	US 95581400	A	19951229	200157 B
			US 96709379	A	19960830	
			US 98170997	A	19981013	
			US 2000586396	A	20000531	

Priority Applications (No Type Date): US 96709379 A 19960830; US 95581400 A 19951229; US 98170997 A 19981013; US 2000586396 A 20000531
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6268749	B1		31	H03L-007/00	CIP of application US 95581400 Div ex application US 96709379 Div ex application US 98170997

Abstract (Basic): US 6268749 B1

NOVELTY - A processor has a first phase locked loop (PLL) with a digital logic portion generating core clock signal. A **level two cache** memory has a second phase locked loop (PLL) whose input is coupled to output of digital logic portion of first PLL. Reset counter provides **synchronization** between phase locked loop after shifting core clock signal.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) Clock generation method;

(b) Clocking circuit

USE - For generating bus clock signal and core clock signals using clock generator fabricated on integrated circuit. Also used for manufacture of digital devices such as discrete logic devices, memory devices, devices either on the same or separate chips, communication devices.

ADVANTAGE - Since single distribution path is provided, skew between the bus clock and core clock signals is reduced. No complex mechanism is needed to maintain **synchronization** . Hence any change in the output of PLL of the processor causes a similar change in the PLL of the **L2** cache memory directly.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of 2/N clocking circuit.

pp; 31 DwgNo 25/26

Title Terms: CLOCK; SIGNAL; GENERATE; SYSTEM; RESET; COUNTER; PHASE; LOCK; LOOP; AFTER; SHIFT; CORE; CLOCK; SIGNAL
Derwent Class: U22; U23
International Patent Class (Main): H03L-007/00
File Segment: EPI

14/5/10 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013990055 **Image available**
WPI Acc No: 2001-474269/200151

Heat-shrinkable polyester-based film

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KOO G H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No Kind Date Applicat No Kind Date Week
KR 2001011260 A 20010215 KR 9930555 A 19990727 200151 B

Priority Applications (No Type Date): KR 9930555 A 19990727
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
KR 2001011260 A 1 G06F-012/00

Abstract (Basic): KR 2001011260 A
NOVELTY - A **2 - level** cache memory system is provided to virtually include a **level 1** cache so that it can implement a DTS for a cache **synchronization** in a multimedia system and reduce a data transmission time.
DETAILED DESCRIPTION - A **2 - level** cache memory system comprises a **level 1** instruction cache(310), a **level 1** data cache(320), a first multiplexor, a second multiplexor, a **level 2** cache(370), a victim buffer(360), a victim controller(390) and a third multiplexor. The **level 1** instruction **cache** (310) stores a **plurality** of instructions connected to tags. The tags are connected by an instruction address bus, and the instructions connected by an instruction bus. The **level 1** data **cache** (320) stores a **plurality** of data connected to the tags. The first multiplexor selectively outputs the tags of the **level 1** instruction cache(310) or the tags of the **level 1** data cache(320) in response to a first selection signal. The second multiplexor selectively the instructions of the **level 1** instruction cache(310) or the data of the **level 1** data cache(320) in response to the first selection signal. The **level 2** cache(370) stores instructions or data connected to the tags. The victim buffer(360) buffers a plurality of victim instructions and data generated from the **level 1** instruction cache(310), the **level 1** data cache(320) or the **level 2** cache(370). The victim controller(390) generates a victim by comparing state bits of the **level 1** instruction cache(310), the **level 1** data cache(320) or the **level 2** cache(370), and transmits the victim data, buffered in the buffer(360), to the **level 2** cache(370) or a main memory.
pp; 1 DwgNo 1/10
Title Terms: HEAT; SHRINK; POLYESTER; BASED; FILM
Derwent Class: T01
International Patent Class (Main): G06F-012/00
File Segment: EPI

14/5/11 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013850791 **Image available**
WPI Acc No: 2001-335004/200135
XRPX Acc No: N01-241795
Multilevel cache system in computer system for handling interactions between queues, has controller logic to control interaction between miss queue and victim queue and write queue buffering
Patent Assignee: SUN MICROSYSTEMS INC (SUNM)
Inventor: MEHROTRA S
Number of Countries: 001 Number of Patents: 001
Patent Family:
Patent No Kind Date Applicat No Kind Date Week
US 6226713 B1 20010501 US 989815 A 19980121 200135 B

Priority Applications (No Type Date): US 989815 A 19980121
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
US 6226713 B1 25 G06F-012/08

Abstract (Basic): US 6226713 B1
NOVELTY - The cache system has a controller logic (502) to control interaction between the miss queue included in a **first level** cache and the victim queue storing entries of a **second level** cache.

DETAILED DESCRIPTION - The cache system has a **first level** cache to receive data access requests from a functional unit in a processor. The **first level** cache includes a miss queue storing entries corresponding to data access requests not received by the **first level** cache. A **second level** cache receives data access requests from a functional unit in the processor. The **first level** cache includes a miss queue, which stores entries corresponding to data access requests not serviced by the **second level** cache. A victim queue stores entries of the **second level** cache which have been evicted from the **second level** cache and a write queue buffering write requests into the **second level** cache. A controller logic (502) controls interaction between the miss queue and the write queue and between the victim queue and the miss queue for processing cache misses. INDEPENDENT CLAIMS are also included for the following:

(a) Processor for executing coded instructions;

(b) Computer system

USE - In computer systems using highly pipelined and superscalar processors for **simultaneously** processing multiple cache system accesses and for handling interactions between the queues of cache levels.

ADVANTAGE - Provides a **multilevel cache** system to access **simultaneously** and handling the interactions between the queues of the cache levels. Is compatible with high speed instruction processing and memory access.

DESCRIPTION OF DRAWING(S) - The figure shows block diagram of the address paths, control logic, and associated queues for a cache memory sub-system.

Controller logic (502)

pp; 25 DwgNo 5/14

Title Terms: MULTILEVEL; CACHE; SYSTEM; COMPUTER; SYSTEM; HANDLE; INTERACT; QUEUE; CONTROL; LOGIC; CONTROL; INTERACT; MISS; QUEUE; VICTIM; QUEUE; WRITING; QUEUE; BUFFER

Derwent Class: T01; U13; U14

International Patent Class (Main): G06F-012/08

International Patent Class (Additional): G06F-013/00

File Segment: EPI

14/5/12 (Item 10 from file: 350)

013499920 **Image available**

WPI Acc No: 2000-671861/200065

XRPX Acc No: N00-498028

Line fill method for interleaving data into level one cache from transition cache by sequencing data packets written to predetermined memory line

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: BORKENHAGEN J M; BROOKHOUSER J I

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6119202	A	20000912	US 97899850	A	19970724	200065	B

Priority Applications (No Type Date): US 97899850 A 19970724

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6119202	A		7	G06F-012/00	

Abstract (Basic): US 6119202 A

NOVELTY - The transition cache (12) data packets are stored in predetermined cache line until they can be forwarded to the **level one** data cache (14). The line fill sequencer (42) controls and manages the flow by continuously looking in transition cache for available packets ready for delivery. Multiple cache lines are interleaved in **parallel** so that, packets from **level two** data **cache** need not wait for a complete line before being written.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also include for a transition cache system for controlling the flow of lines of data.

USE - For interleaving data into **level one** cache from transition cache.

ADVANTAGE - It delivers data to a **level one** data cache from a transition cache at different speeds from different devices.

DESCRIPTION OF DRAWING(S) - The figure shows a block diagram of a computer system for interleaving line fill.

Transition Cache (12)

Level One Data cache (14)

Line fill Sequencer (42)

pp; 7 DwgNo 1/3

Title Terms: LINE; FILL; METHOD; INTERLEAVED; DATA; LEVEL; ONE; CACHE; TRANSITION; CACHE; SEQUENCE; DATA; PACKET; WRITING; PREDETERMINED; MEMORY ; LINE

Derwent Class: T01

International Patent Class (Main): G06F-012/00

File Segment: EPI

14/5/13 (Item 11 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013421322 **Image available**

WPI Acc No: 2000-593261/200056

XRPX Acc No: N00-439282

Processor bus traffic optimization method for multi - level cache , **involves setting reflection status bit to zero, when no valid copy of address is received from system bus snoop cycle**

Patent Assignee: UNISYS CORP (BURS)

Inventor: WHITTAKER B E

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6070233	A	20000530	US 96592093	A	19960126	200056 B
			US 97931329	A	19970916	

Priority Applications (No Type Date): US 96592093 A 19960126; US 97931329 A 19970916

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6070233	A		17	G06F-013/14	Cont of application US 96592093

Abstract (Basic): US 6070233 A

NOVELTY - The status bit R is set to 0, when no valid copy of address is received from system bus snoop cycle. When R-bit status value for address in **second level** cache unit is set to 0, V is set to 0. The address received from system bus snoop cycle is then transferred to **first level** cache unit.

DETAILED DESCRIPTION - A system bus snoop cycle is initiated to retrieve address of modified data. The addresses are then loaded in an individual queue, for subsequent invalidation of addresses in cache units. Status bits (V,R) for each address in **second level** cache unit is set to indicate validity V=1, invalidity V=0. The **first level** cache unit has a valid copy of cache address, when R=1, and no valid copy of each address, when R=0. Snare gates in programmable logic array unit is utilized as a single cache controller for first and **second** logic **level** cache units. When an address received from system bus snoop cycle matches an address in **second level** cache units, each address in **second** logic **level** is invalidated by setting V=0. When an address from system bus snoop cycle matches the address in **second level** cache unit, the R-bit status value is checked.

USE - For optimizing processor bus traffic in **multi - level cache** which utilizes reflection status bit to indicate data inclusion in higher level cache.

ADVANTAGE - **Two level caches** operate in **synchronization** , since the **second level** cache always knows the status of address

data in first cache, by excluding use of internal processing bus, thereby speeding-up processor operation. Enhances cache hit rate by 5-10% without need for including any extra hardware.

DESCRIPTION OF DRAWING(S) - The figure shows the flowchart indicating steps involved in invalidation cycle with use of newly added reflection status bit (R bit).

pp; 17 DwgNo 1/9

Title Terms: PROCESSOR; BUS; TRAFFIC; METHOD; MULTI; LEVEL; CACHE; SET; REFLECT; STATUS; BIT; ZERO; NO; VALID; COPY; ADDRESS; RECEIVE; SYSTEM; BUS; CYCLE

Derwent Class: T01

International Patent Class (Main): G06F-013/14

File Segment: EPI

14/5/14 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

013376721 **Image available**

WPI Acc No: 2000-548659/200050

XRPX Acc No: N00-405916

Two - level cache **memory for computers, comprises** two cache **with** different levels **coupled by queuing structure,** caches **being** dual **ported**

Patent Assignee: INTEL CORP (ITLC)

Inventor: FU J W C; MATHEWS G S; MULLA D A; SAILER S E; MATTHEWS G

Number of Countries: 091 Number of Patents: 008

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200039764	A1	20000706	WO 99US31179	A	19991229	200050	B
AU 200022205	A	20000731	AU 200022205	A	19991229	200050	
US 6272597	B1	20010807	US 98223847	A	19981231	200147	
GB 2359910	A	20010905	WO 99US31179	A	19991229	200152	
			GB 200112694	A	20010524		
DE 19983859	T	20020228	DE 1083859	A	19991229	200223	
			WO 99US31179	A	19991229		
CN 1333906	A	20020130	CN 99815362	A	19991229	200231	
TW 454161	A	20010911	TW 99121954	A	19991215	200242	
GB 2359910	B	20031217	WO 99US31179	A	19991229	200404	
			GB 200112694	A	20010524		

Priority Applications (No Type Date): US 98223847 A 19981231

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200039764	A1	E	30	G08B-005/22	

Designated States (National): AE AL AM AT AU AZ BA BB BG BR BY CA CH CN CR CU CZ DE DK DM EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW

Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW

AU 200022205	A		Based on patent WO 200039764
US 6272597	B1	G06F-012/10	
GB 2359910	A	G06F-012/08	Based on patent WO 200039764
DE 19983859	T	G08B-005/22	Based on patent WO 200039764
CN 1333906	A	G08B-005/22	
TW 454161	A	G08B-005/22	
GB 2359910	B	G06F-012/08	Based on patent WO 200039764

Abstract (Basic): WO 200039764 A1

NOVELTY - The memory comprises **caches** (110,120) of **different levels** (L0, **L1**) that are adapted to contain integer data, and both integer data and floating point data, respectively. The caches are dual ported so that a 64 bit virtual address is **simultaneously** received at both address ports.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) microprocessor chip;
(b) cache memory accessing method
USE - For computers.
ADVANTAGE - The microprocessor performance increases by provision of the **two level cache** memory, the **two levels** being optimized for low latency and capacity, respectively.
DESCRIPTION OF DRAWING(S) - The figure shows block diagram of cache memory.
Caches (110,120)
Levels (L0, **L1**)
pp; 30 DwgNo 1/6

Title Terms: TWO; LEVEL; CACHE; MEMORY; COMPUTER; COMPRISE; TWO; CACHE; LEVEL; COUPLE; QUEUE; STRUCTURE; DUAL; PORT
Derwent Class: T01
International Patent Class (Main): G06F-012/08; G06F-012/10; G08B-005/22
International Patent Class (Additional): H04B-007/00
File Segment: EPI

14/5/15 **(Item 13 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

011492478 **Image available**
WPI Acc No: 1997-470391/199743
XRPX Acc No: N97-392519
Two - level **virtual-real set-associative** cache **system for detecting and resolving synonyms - tags** 1st level **virtual cache lines with virtual address and real pointer to corresp line in** 2nd level **real cache, whose lines are tagged with real address and virtual pointer to corresp line in** 1st level **virtual cache**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: WU C E
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 5668968	A	19970916	US 92844812	A	19920302	199743 B
			US 94345802	A	19941122	

Priority Applications (No Type Date): US 92844812 A 19920302; US 94345802 A 19941122
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5668968	A		134	G06F-012/10	Cont of application US 92844812

Abstract (Basic): US 5668968 A
Lines of a **first level** virtual cache are tagged with a virtual address and a real pointer which points to a corresponding line in a **second level** real cache. Lines in the **second level** real cache are tagged with a real address and a virtual pointer which points to a corresponding line in the **first level** virtual cache, if one exists. A translation-look-aside buffer (TLB) is used for translating virtual to real addresses for accessing the **second level** real cache. Synonym detection is performed at the **second level** real cache.
An inclusion bit I is set in a directory of the **second level** real cache to indicate that a particular line is included in the **first level** virtual cache. Another bit, called a buffer bit B, is set whenever a line in the **first level** virtual cache is placed in a **first level** virtual cache write-back buffer for updating main memory. When a **first level** cache miss occurs, the TLB generates a corresponding real address for that page and the **first level** virtual cache selects a line for replacement and also notifies the **second level** real cache which line it chooses for replacement. The real address is then used to access the **second level** real cache. Synonym detection and resolution are performed by the **second level** real cache.
ADVANTAGE - Provides **parallel** access to TLB and **L1** cache and solves synonym problems without requiring reverse translation table.

little hardware overhead for solving synonym problems usually associated with virtual address caches.

Dwg.1/3

Title Terms: TWO; LEVEL; VIRTUAL; REAL; SET; ASSOCIATE; CACHE; SYSTEM; DETECT; RESOLUTION; TAG; LEVEL; VIRTUAL; CACHE; LINE; VIRTUAL; ADDRESS; REAL; POINT; CORRESPOND; LINE; LEVEL; REAL; CACHE; LINE; TAG; REAL; ADDRESS; VIRTUAL; POINT; CORRESPOND; LINE; LEVEL; VIRTUAL; CACHE

Derwent Class: T01

International Patent Class (Main): G06F-012/10

International Patent Class (Additional): G06F-012/08

File Segment: EPI

14/5/16 **(Item 14 from file: 350)**

DIALOG(R)File 350:Derwent WPIX

010865387 **Image available**

WPI Acc No: 1996-362338/199636

Related WPI Acc No: 1994-135069; 1998-051794

Two - level cache memory system for computer system using e.g. commodity dynamic RAM - has two primary cache memories being accessed by virtual addressing to store data and instruction and secondary cache memory using TLB translated physical address to store both instruction and data

Patent Assignee: SILICON GRAPHICS INC (SILI-N)

Inventor: FARMWALD P M; LAYMAN T P; NGO H X; ROBERTS A W; TAYLOR G S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5542062	A	19960730	US 89444660	A	19891201	199636	B
			US 9359715	A	19930510		
			US 93172684	A	19931222		

Priority Applications (No Type Date): US 89444660 A 19891201; US 9359715 A 19930510; US 93172684 A 19931222

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5542062	A		20	G06F-012/08	Cont of application US 89444660
					Cont of application US 9359715
					Cont of patent US 5307477

Abstract (Basic): US 5542062 A

The **cache** memory system includes a processor, **two** primary **level caches**, and a **secondary level cache**. The **two** primary **level caches**, e.g. direct mapped, are coupled to the processor for storing instructions and they are accessible by the processor using a virtual addressing scheme. The processor also transmits virtual addresses to the **two** primary **level caches** within an initial time period to eliminate the need for address translation to access the caches.

The **secondary level** cache is coupled to the processor for storing instructions and data and is accessible by the processor which transmits physical addresses to the **secondary level** cache within a second time period. This second time period is greater than the initial time period and the **secondary level cache** is larger that the **two** primary **level caches**. The physical addresses are generated using only a partial TLB translation to provide full access to the cache memory system without full width TLB translation.

USE/ADVANTAGE - For processor having extremely fast clock speed. Secondary cache reference can be started **simultaneously** as primary cache reference whenever secondary cache is not busy completing previous transaction. Only if ''miss'' is encountered in primary and secondary caches does processor access main memory.

Dwg.1/16

Title Terms: TWO; LEVEL; CACHE; MEMORY; SYSTEM; COMPUTER; SYSTEM; COMMODITY; DYNAMIC; RAM; TWO; PRIMARY; CACHE; MEMORY; ACCESS; VIRTUAL; ADDRESS;

STORAGE; DATA; INSTRUCTION; SECONDARY; CACHE; MEMORY; TLB; TRANSLATION; PHYSICAL; ADDRESS; STORAGE; INSTRUCTION; DATA
Index Terms/Additional Words: TRANSLATION; LOOKASIDE; BUFFER
Derwent Class: T01
International Patent Class (Main): G06F-012/08
File Segment: EPI

14/5/17 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010523768 **Image available**
WPI Acc No: 1996-020721/199602
XRPX Acc No: N96-017200

Integrated level two cache and main memory controller - has storage controller with L2 directory to compare address of data in cache with desired information address to determine occurrence of cache hit or miss and provides data directly to processor via unique ports of cache and memory

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC); IBM CORP (IBMC); IBM DEUT INFORMATIONSSYSTEME GMBH (IBMC)
Inventor: SHIPPY D J; SHULER D B
Number of Countries: 029 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9532472	A1	19951130	WO 94EP4315	A	19941227	199602	B
JP 7319767	A	19951208	JP 95111435	A	19950510	199607	
BR 9502022	A	19960130	BR 952022	A	19950511	199612	
CA 2142799	A	19951120	CA 2142799	A	19950217	199613	
EP 760133	A1	19970305	WO 94EP4315	A	19941227	199714	
			EP 95905594	A	19941227		
CN 1123933	A	19960605	CN 95106102	A	19950509	199747	
HU 76241	T	19970728	WO 94EP4315	A	19941227	199809	
			HU 963142	A	19941227		
US 6226722	B1	20010501	US 94245786	A	19940519	200126	
CZ 9603197	A3	20020612	WO 94EP4315	A	19941227	200251	
			CZ 963197	A	19941227		

Priority Applications (No Type Date): US 94245786 A 19940519
Cited Patents: 2.Jnl.Ref; GB 2011678
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9532472	A1	E	35	G06F-012/08	
Designated States (National): BY CZ HU PL RU SK UA					
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE					
JP 7319767	A		18	G06F-012/08	
BR 9502022	A			G06F-012/00	
CA 2142799	A			G06F-013/20	
EP 760133	A1	E	35	G06F-012/08	Based on patent WO 9532472
Designated States (Regional): AT BE CH DE ES FR GB IT LI NL SE					
CN 1123933	A			G06F-015/00	
HU 76241	T			G06F-012/08	Based on patent WO 9532472
US 6226722	B1			G06F-012/08	
CZ 9603197	A3			G06F-012/08	Based on patent WO 9532472

Abstract (Basic): WO 9532472 A

The computer system includes a processing unit, external **L2** cache and memory. A storage controller (SC) controls access between the CPU, the **L2** cache and main memory. The SC includes a **L2** directory to compare a address of the data or instruction in the cache with the address of the desired information to determine if a cache hit or miss has occurred.

The SC provides address and control information to **L2** and memory. The data retrieval is **simultaneously** initiated in both **L2** cache and main memory. The **L2** cache passes data or instruction directly to the processing unit which has requested information. Both the external

cache and the memory have a unique port to allow direct data transfer into the processing unit.

ADVANTAGE - Allows memory latency associated with arbitration, and memory DRAM address translation to be minimised in event that data sought by processor is not in **L2** cache. Eliminates overhead associated with storing the in intermediate device such as cache or memory controller.

Dwg.2/8

Title Terms: INTEGRATE; LEVEL; TWO; CACHE; MAIN; MEMORY; CONTROL; STORAGE; CONTROL; DIRECTORY; COMPARE; ADDRESS; DATA; CACHE; INFORMATION; ADDRESS; DETERMINE; OCCUR; CACHE; HIT; MISS; DATA; PROCESSOR; UNIQUE; PORT; CACHE; MEMORY

Derwent Class: T01

International Patent Class (Main): G06F-012/00; G06F-012/08; G06F-013/20; G06F-015/00

File Segment: EPI

14/5/18 (Item 16 from file: 350)

009857404 **Image available**

WPI Acc No: 1994-137260/199417

Related WPI Acc No: 1998-597050

XRPX Acc No: N94-107827

Bi-level data compression appts. with synchronously **operating cache memories - determines if received data segment is found in cache memory and if not assigns segment to cache memory's** first level **and assigns that segment to less recently used** second level

Patent Assignee: HEWLETT-PACKARD CO (HEWP)

Inventor: BERGE T G; ROSENBURG C J; ROSENBERG C

Number of Countries: 008 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 593968	A1	19940427	EP 93116015	A	19931004	199417	B
JP 6242924	A	19940902	JP 93283976	A	19931018	199440	
US 5450562	A	19950912	US 92963201	A	19921019	199542	
EP 593968	B1	20000614	EP 93116015	A	19931004	200033	
			EP 98113104	A	19931004		
DE 69328855	E	20000720	DE 628855	A	19931004	200041	
			EP 93116015	A	19931004		
SG 75758	A1	20001024	SG 961806	A	19931004	200060	
KR 319657	B	20020406	KR 9321597	A	19931018	200267	

Priority Applications (No Type Date): US 92963201 A 19921019

Cited Patents: 2.Jnl.Ref; EP 491498; GB 2214669; US 4562536

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 593968	A1	E	20	G06F-012/12	
Designated States (Regional): DE FR GB IT					
JP 6242924	A		14	G06F-005/00	
US 5450562	A		16	G06F-012/02	
EP 593968	B1	E		G06F-012/12	Related to application EP 98113104
					Related to patent EP 880100
Designated States (Regional): DE FR GB IT					
DE 69328855	E			G06F-012/12	Based on patent EP 593968
SG 75758	A1			G06F-012/12	
KR 319657	B			G06F-012/08	Previous Publ. patent KR 94009841

Abstract (Basic): EP 593968 A

The appts. has a cache memory (66) with levels for a most recently used data segment and less recently used data segments. It determines (62) if received segment is found in first cache memory, assigns data there and assigns previously received data segment to a position in **second level** in less recently used area using pseudo-random method.

Transmits (62) to a receiving 'not found' area an indication the received data segment in uncompressed format. In response to the

determination that the received segment is found in the first cache transmits a position code indicating where in the first cache the data segment is assigned, using a compressed form of the received data.

ADVANTAGE - Provides cache based compression and decompression procedure which is more efficient through use of improved cache management techniques.

Dwg.4/14

Title Terms: DATA; COMPRESS; APPARATUS; **SYNCHRONOUS** ; OPERATE; CACHE; MEMORY; DETERMINE; RECEIVE; DATA; SEGMENT; FOUND; CACHE; MEMORY; ASSIGN; SEGMENT; CACHE; MEMORY; FIRST; LEVEL; ASSIGN; SEGMENT; LESS; RECENT; SECOND; LEVEL

Derwent Class: T01; U21

International Patent Class (Main): G06F-005/00; G06F-012/02; G06F-012/08; G06F-012/12

International Patent Class (Additional): G06F-012/10; H03M-007/30; H04N-001/417

File Segment: EPI

14/5/19 **(Item 17 from file: 350)**

0019455213 **Image available**

WPI Acc No: 1994-135069/199416

Related WPI Acc No: 1996-362338; 1998-051794

XRPX Acc No: N94-106203

Two level cycle cache memory system - has processor for generating virtual address, prim cache memory contg prim cache tag devices, prom instruction cache device and prim data cache device

Patent Assignee: MIPS COMPUTER SYSTEMS INC (MIPS-N)

Inventor: FARMWALD P M; LAYMAN T P; NGO H X; ROBERTS A W; TAYLOR G S

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5307477	A	19940426	US 89444660	A	19891201	199416	B
			US 9359715	A	19930510		

Priority Applications (No Type Date): US 89444660 A 19891201; US 9359715 A 19930510

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5307477	A		20	G06F-012/08	Cont of application US 89444660

Abstract (Basic): US 5307477 A

A **two - level cache** memory system for use in a computer system including two primary cache memories, one for storing instructions and one for storing data. The system also includes a secondary cache memory for storing both instructions and data. The primary and secondary caches each employ their own separate tag directory. The primary caches use a virtual addressing scheme employing both virtual tags and virtual addresses. The secondary cache employs a hybrid addressing scheme which uses virtual tags and partial physical addresses.

The primary and secondary caches operate in **parallel** unless the larger and slower secondary cache is busy performing a previous operation. Only if a ''miss'' is encountered in both the primary and secondary caches does the system processor access the main memory.

USE/ADVANTAGE - As **two - level cache** memory system, with **separate** prim instruction and data **caches** and single sec cache contg both instruction and data. Provision for overcome large ration of memory access time to processor cycle time.

Dwg.1/16

Title Terms: TWO; LEVEL; CYCLE; CACHE; MEMORY; SYSTEM; PROCESSOR; GENERATE; VIRTUAL; ADDRESS; PRIMARY; CACHE; MEMORY; CONTAIN; PRIMARY; CACHE; TAG; DEVICE; PROM; INSTRUCTION; CACHE; DEVICE; PRIMARY; DATA; CACHE; DEVICE

Derwent Class: T01

International Patent Class (Main): G06F-012/08

File Segment: EPI

14/5/20 **(Item 18 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

009150283 **Image available**
WPI Acc No: 1992-277721/199234
XRPX Acc No: N92-212407
Multiple level caches for multiprocessor system - provides on-chip L1 caches interfaced with external L2 caches, with D2 directories parallel to L2 caches which shadow L1 caches to maintain data coherence
Patent Assignee: IBM CORP (IBMC)
Inventor: SO K; WANG W H
Number of Countries: 000 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 481233	A	19920422				199234	B
EP 481233	A3	19920429	EP 91115825	A	19910918	199329	

Priority Applications (No Type Date): US 90597902 A 19901012
Cited Patents: 1.Jnl.Ref; EP 243724; EP 278196; US 4675811
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 481233	A		30		

Abstract (Basic): EP 481233 A

The system comprises a directory (D) interposed between the cache (**L1**) and a next higher level of cache storage (**L2**), which determines whether data lines are within the cache. The directory indicates whether the data lines are shared by other memory locations of the multiprocessor system. The cache indicates whether data lines in the cache have been changed. The system can operate without enforcement of an inclusion property between the cache and the next higher level of cache storage.

The directory indicates whether data lines in the internal cache have been changed. The next higher level of cache is shared by at least one other processor (MPU) of the multiprocessor system.

ADVANTAGE - The MPUs perform at high speeds and permit the further coupling of additional MPUs to the multiprocessor system.

Dwg.6/16

Title Terms: MULTIPLE; LEVEL; MULTIPROCESSOR; SYSTEM; INTERFACE; EXTERNAL; DIRECTORY; **PARALLEL** ; SHADOW; MAINTAIN; DATA; COHERE
Derwent Class: T01
International Patent Class (Additional): G06F-012/08
File Segment: EPI

14/5/21 **(Item 19 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

008777632 **Image available**
WPI Acc No: 1991-281649/199138
XRPX Acc No: N91-215271
Branch prediction cache structure responds to input program counter - using two levels that respond to both small and large entry numbers
Patent Assignee: NEXGEN MICROSYSTEMS (NEXG-N); NEXGEN INC (NEXG-N); ADVANCED MICRO DEVICES INC (ADMI); NEXGEN MICROSYST (NEXG-N)
Inventor: FAVOR J G; STILES D R; VAN DYKE K S; VANDYKE K
Number of Countries: 016 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9113402	A	19910905				199138	B
US 5163140	A	19921110	US 90485306	A	19900226	199248	
			US 92844995	A	19920302		
US 5327547	A	19940705	US 90485306	A	19900226	199426	
			US 92844995	A	19920302		
			US 92954441	A	19920930		

US 5515518	A	19960507	US 90485306	A	19900226	199624
			US 92844995	A	19920302	
			US 92954441	A	19920930	
			US 94270855	A	19940705	
US 6067616	A	20000523	US 90485306	A	19900226	200032
			US 92844995	A	19920302	
			US 92954441	A	19920930	
			US 94270855	A	19940705	
			US 96638389	A	19960426	
US 6425075	B1	20020723	US 90485306	A	19900226	200254
			US 92844995	A	19920302	
			US 92954441	A	19920930	
			US 94270855	A	19940705	
			US 96638389	A	19960426	
			US 99361809	A	19990727	

Priority Applications (No Type Date): US 90485306 A 19900226; US 92844995 A 19920302; US 92954441 A 19920930; US 94270855 A 19940705; US 96638389 A 19960426; US 99361809 A 19990727
Cited Patents: NoSR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9113402	A				
Designated States (National): DE GB JP KR					
Designated States (Regional): AT BE CH DK ES FR GB GR IT LU NL SE					
US 5163140	A		19	G06F-012/00	Cont of application US 90485306
US 5327547	A		20	G06F-012/08	Cont of application US 90485306
					Cont of application US 92844995
					Cont of patent US 5163140
US 5515518	A		20	G06F-009/30	Cont of application US 90485306
					Cont of application US 92844995
					Cont of application US 92954441
					Cont of patent US 5163140
					Cont of patent US 5327547
US 6067616	A			G06F-009/30	Cont of application US 90485306
					Cont of application US 92844995
					Cont of application US 92954441
					Cont of application US 94270855
					Cont of patent US 5163140
					Cont of patent US 5327547
					Cont of patent US 5515518
US 6425075	B1			G06F-012/00	Cont of application US 90485306
					Cont of application US 92844995
					Cont of application US 92954441
					Cont of application US 94270855
					Div ex application US 96638389
					Cont of patent US 5163140
					Cont of patent US 5327547
					Cont of patent US 5515518
					Div ex patent US 6067616

Abstract (Basic): WO 9113402 A

The branch prediction cache (BPC) structure responds to an input program counter (PC). It includes two levels of BPC: one responds to part of the PC input this has a small number of entries and the other has a large number entries. The entries correspond to previously encountered branch instructions.

The **first level** BPC has an entry providing almost full prediction capability while the **second level** BPC has an entry providing almost linked prediction capability regarding their associated branch instructions.

USE - Cache structures in computer systems that aid prediction of conditional and unconditional branches. (32pp Dwg.No.2/1

Title Terms: BRANCH; PREDICT; CACHE; STRUCTURE; RESPOND; INPUT; PROGRAM; COUNTER; TWO; LEVEL; RESPOND; ENTER; NUMBER
Derwent Class: T01
International Patent Class (Main): G06F-009/30; G06F-012/00; G06F-012/08
International Patent Class (Additional): G06F-009/38; G06F-013/00

File Segment: EPI

14/5/22 **(Item 20 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

008315415 **Image available**
WPI Acc No: 1990-202416/199027
XRPX Acc No: N90-157550

Multiprocessor system for storage buffers for each processor - has buffers located between each processor and common memory and provide buffering for writing in to common memory

Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: GUSEFSKI R J; LEI C I; RAMIREZ A
Number of Countries: 004 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 375892	A	19900704	EP 90120600	A	19901107	199027	B
US 5202972	A	19930413	US 88291805	A	19881229	199317	
			US 91725919	A	19910703		
EP 375892	B1	19960717	EP 89120600	A	19891107	199633	
DE 68926850	E	19960822	DE 626850	A	19891107	199639	
			EP 89120600	A	19891107		

Priority Applications (No Type Date): US 88291805 A 19881229; US 91725919 A 19910703
Cited Patents: 3.Jnl.Ref; A3...9142; EP 149392; NoSR.Pub
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5202972	A		18	G06F-013/00	Cont of application US 88291805
EP 375892	B1	E	22	G06F-012/08	
Designated States (Regional): DE FR GB					
DE 68926850	E			G06F-012/08	Based on patent EP 375892

Abstract (Basic): EP 375892 A

Data instructions caches are provided for each processor (20) and buffer storage (27) is provided between each processor and the common memory (10). Data is written by a processor to the buffer storage in **parallel** with the caches, but writes data to the master storage sequentially as directed by the master storage controller unit. Each storage buffer contains eight entries where each entry includes an effective and an absolute address, status bits and a data portion including white flags.

Status bits indicate which instruction the data relates to and whether or not the data has been written to master storage. Other status bits indicate whether the entry is for a sequential or a non-sequential write operation.

ADVANTAGE - Improves processing speed by avoiding delaying processors while writing to main storage. (20pp Dwg.No.4/8

Title Terms: MULTIPROCESSOR; SYSTEM; STORAGE; BUFFER; PROCESSOR; BUFFER; LOCATE; PROCESSOR; COMMON; MEMORY; BUFFER; WRITING; COMMON; MEMORY
Derwent Class: T01
International Patent Class (Main): G06F-012/08; G06F-013/00
International Patent Class (Additional): G06F-009/00; G06F-015/16
File Segment: EPI